

# DATA SHEET

## **74AHC2G00; 74AHCT2G00** 2-input NAND gate

Product specification

2004 Jan 21

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

## FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 500 V.
- Low power dissipation
- Balanced propagation delays
- SOT505-2 and SOT765-1 package
- Specified from –40 to +85 °C and –40 to +125 °C.

## DESCRIPTION

The 74AHC2G/AHCT2G00 is a high-speed Si-gate CMOS device.

The 74AHC2G/AHCT2G00 provides the 2-input NAND gate function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC2G	AHCT2G	
$t_{PHL}/t_{PLH}$	propagation delay nA and nB to nY	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	3.5	3.6	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance per gate	$C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2	17	18	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC2G00DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	A00
74AHCT2G00DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	C00
74AHC2G00DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	A00
74AHCT2G00DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	C00

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	2B	data input
7	1Y	data output
8	V <sub>CC</sub>	supply voltage

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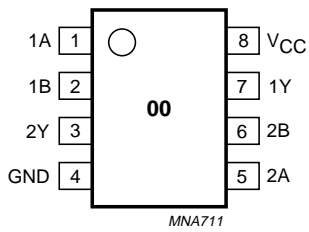


Fig.1 Pin configuration.

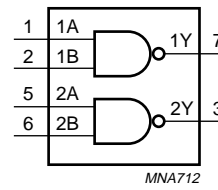


Fig.2 Logic symbol.

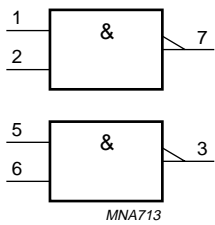


Fig.3 IEC logic symbol.

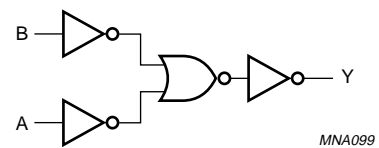


Fig.4 Logic diagram.

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC2G00			74AHCT2G00			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	5.5	0	–	5.5	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 3.3 \pm 0.3$ V	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \pm 0.5$ V	–	–	20	–	–	20	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$V_I$	input voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5$ V	–	–20	mA
$I_{OK}$	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
$I_O$	output source or sink current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V	–	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		–	±75	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_D$	power dissipation	$T_{amb} = -40$ to $+125$ °C	–	250	mW

## Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 2-input NAND gate

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## DC CHARACTERISTICS

## Type 74AHC2G00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –50 µA	2.0	1.9	2.0	–	V
		I <sub>O</sub> = –50 µA	3.0	2.9	3.0	–	V
		I <sub>O</sub> = –50 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4.0 mA	3.0	2.58	–	–	V
		I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA	2.0	–	0	0.1	V
		I <sub>O</sub> = 50 µA	3.0	–	0	0.1	V
		I <sub>O</sub> = 50 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.36	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.36	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	µA
C <sub>I</sub>	input capacitance		–	–	1.5	10	pF

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 µA	2.0	1.9	–	–	V
		I <sub>O</sub> = -50 µA	3.0	2.9	–	–	V
		I <sub>O</sub> = -50 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	3.0	2.48	–	–	V
		I <sub>O</sub> = -8.0 mA	4.5	3.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA	2.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA	3.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.44	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.44	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	µA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 µA	2.0	1.9	–	–	V
		I <sub>O</sub> = -50 µA	3.0	2.9	–	–	V
		I <sub>O</sub> = -50 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	3.0	2.40	–	–	V
		I <sub>O</sub> = -8.0 mA	4.5	3.70	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA	2.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA	3.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	2.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	40	µA
C <sub>I</sub>	input capacitance		–	–	–	10	pF



## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

**Type 74AHCT2G00**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –50 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.36	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.35	mA
C <sub>I</sub>	input capacitance			–	1.5	10	pF
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –50 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –8.0 mA	4.5	3.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.44	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5	4.4	–	–	V
		I <sub>O</sub> = -50 µA I <sub>O</sub> = -8.0 mA	4.5	3.70	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5	–	–	0.1	V
		I <sub>O</sub> = 50 µA I <sub>O</sub> = 8.0 mA	4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	2.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

## AC CHARACTERISTICS

## Type 74AHC2G00

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$C_L$ (pF)	$V_{CC}$ (V)				
<b><math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	3.0 to 3.6	–	4.5 <sup>(1)</sup>	7.9	ns
				4.5 to 5.5	–	3.5 <sup>(2)</sup>	5.5	ns
		50	3.0 to 3.6	–	6.5 <sup>(1)</sup>	11.4	ns	
			4.5 to 5.5	–	4.9 <sup>(2)</sup>	7.5	ns	
<b><math>T_{amb} = -40\text{ to }+85\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	3.0 to 3.6	1.0	–	9.5	ns
				4.5 to 5.5	1.0	–	6.5	ns
		50	3.0 to 3.6	1.0	–	13.0	ns	
			4.5 to 5.5	1.0	–	8.5	ns	
<b><math>T_{amb} = -40\text{ to }+125\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	3.0 to 3.6	1.0	–	10.5	ns
				4.5 to 5.5	1.0	–	7.0	ns
		50	3.0 to 3.6	1.0	–	14.5	ns	
			4.5 to 5.5	1.0	–	9.5	ns	

## Notes

1. Typical values are measured at  $V_{CC} = 3.3$  V.
2. Typical values are measured at  $V_{CC} = 5.0$  V.

## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

**Type 74AHCT2G00**GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

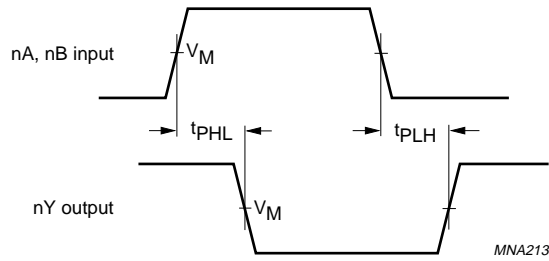
SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$C_L$ (pF)	$V_{CC}$ (V)				
<b><math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	4.5 to 5.5	1.0	3.6 <sup>(1)</sup>	6.2	ns
			50	4.5 to 5.5	1.0	5.0 <sup>(1)</sup>	7.9	ns
<b><math>T_{amb} = -40\text{ to }+85\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	4.5 to 5.5	1.0	–	7.1	ns
			50	4.5 to 5.5	1.0	–	9.0	ns
<b><math>T_{amb} = -40\text{ to }+125\text{ }^\circ\text{C}</math></b>								
$t_{PHL}/t_{PLH}$	propagation delay input nA and nB to output nY	see Figs 5 and 6	15	4.5 to 5.5	1.0	–	8.0	ns
			50	4.5 to 5.5	1.0	–	10.0	ns

**Note**1. Typical values are measured at  $V_{CC} = 5.0$  V.

2-input NAND gate

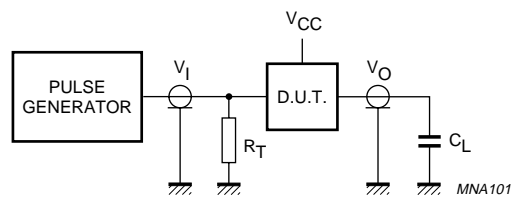
74AHC2G00; 74AHCT2G00

AC WAVEFORMS



FAMILY	V <sub>M</sub> INPUT	V <sub>M</sub> OUTPUT
AHC2G00	50% V <sub>CC</sub>	50% V <sub>CC</sub>
AHCT2G00	1.5 V	50% V <sub>CC</sub>

Fig.5 The inputs (nA and nB) to output (nY) propagation delays.



FAMILY	V <sub>I</sub> INPUT REQUIREMENTS
AHC2G00	GND to V <sub>CC</sub>
AHCT2G00	GND to 3.0 V

Definitions for test circuit:

C<sub>L</sub> = Load capacitance including jig and probe capacitance (See "AC characteristics" for the value).

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>0</sub> of the pulse generator.

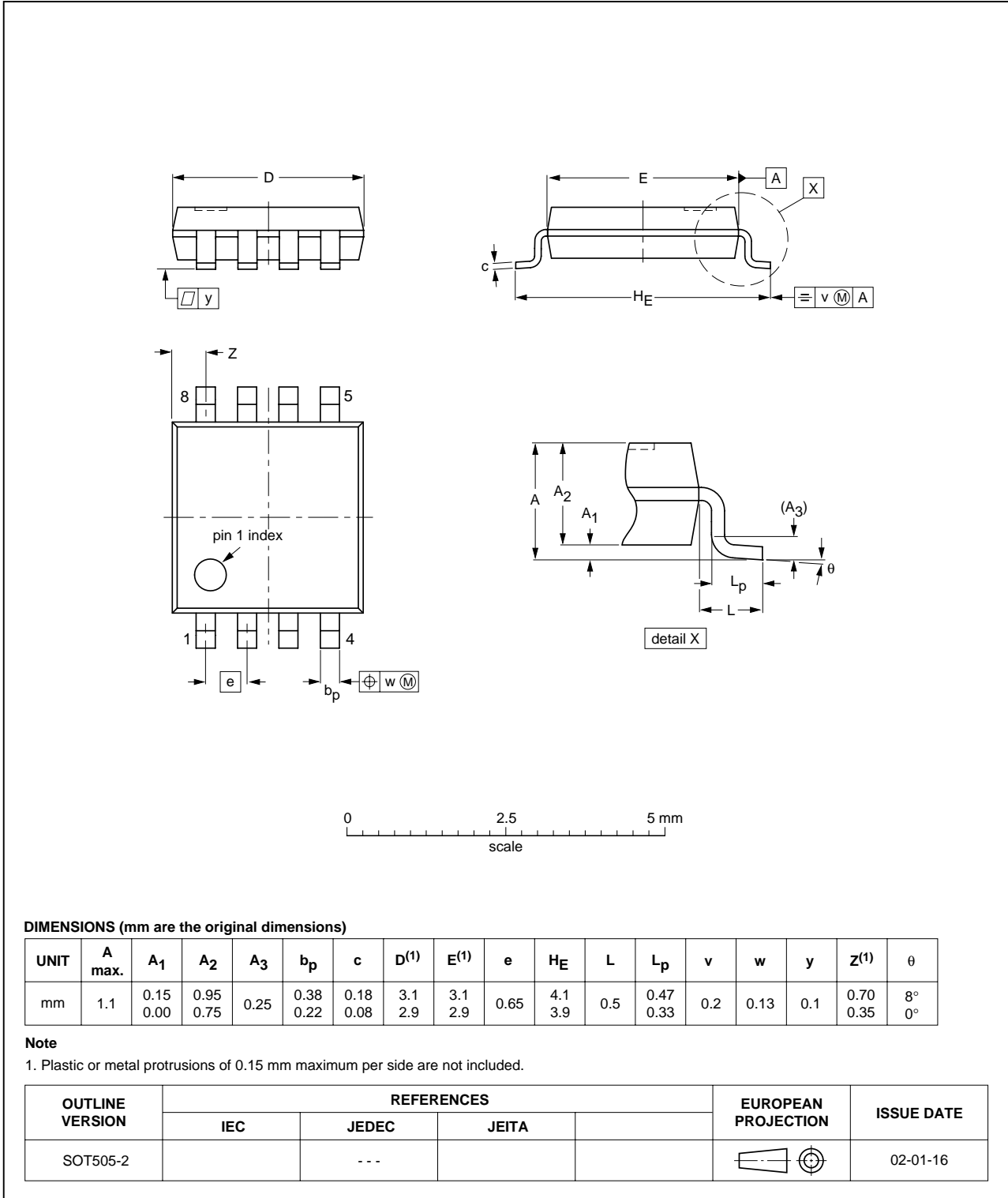
Fig.6 Load circuitry for switching times.

2-input NAND gate

74AHC2G00; 74AHCT2G00

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

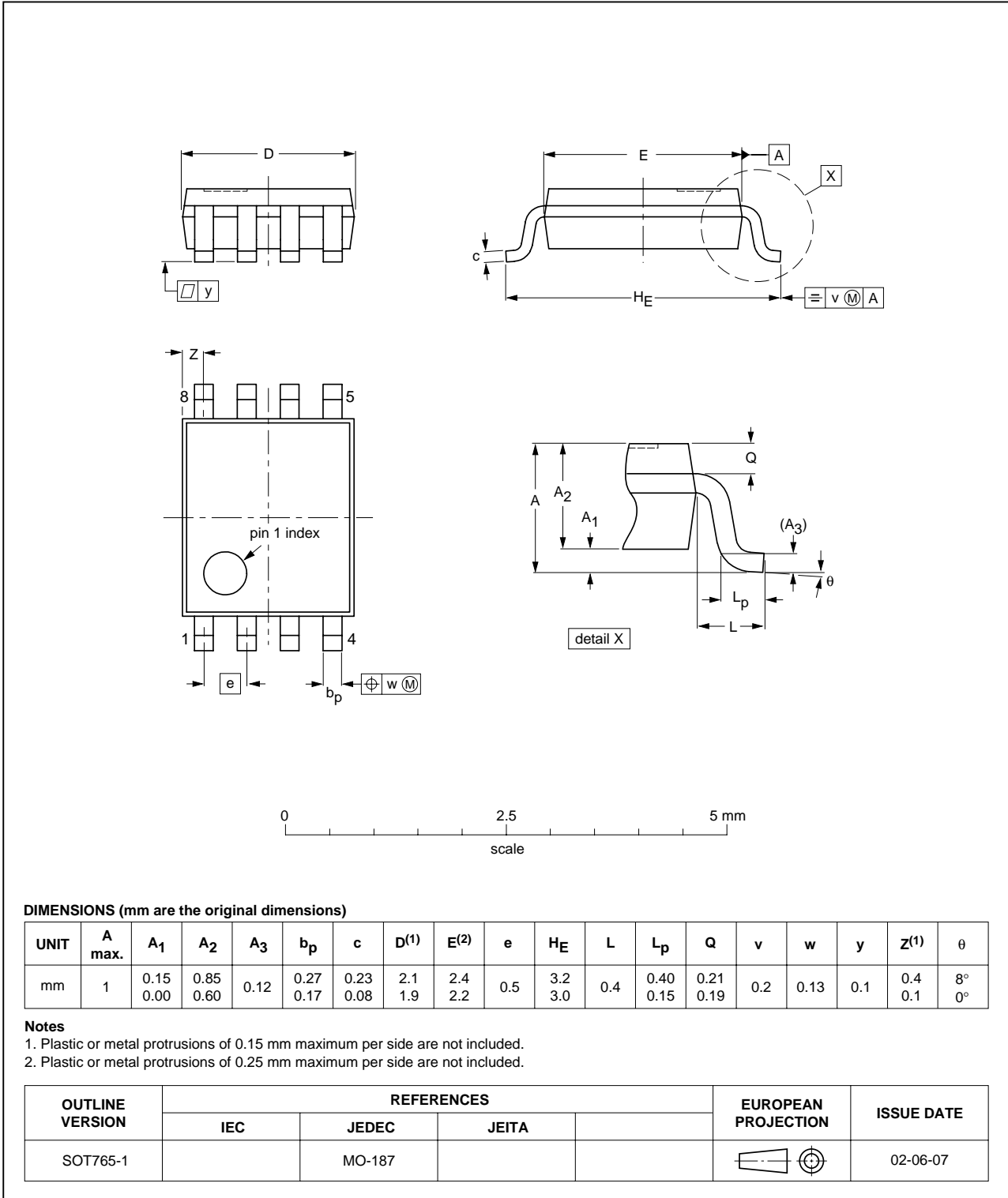


2-input NAND gate

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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



## 2-input NAND gate

## 74AHC2G00; 74AHCT2G00

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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## Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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